



Attorney Docket No.: CYPR-CD01208

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Patent Application

Inventor(s): Craig Nemecek

Application No.: 09/989,777

Group Art Unit:

Filed: 11/19/01

Examiner:

Title: SLEEP AND STALL IN AN IN-CIRCUIT EMULATION SYSTEM

Form 1449

U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
<i>Appl</i>	A	6,144,327	11/07/00	Distinti et al.	341	126	08/12/97
<i>Appl</i>	B	5,202,687	04/13/93	Distinti	341	158	06/12/91
<i>Appl</i>	C	6,016,554	01/18/00	Skrovan et al.	741	25	07/28/97
<i>Appl</i>	D	5,978,584	11/02/99	Nishibata et al.	395	704	06/19/97
<i>Appl</i>	E	6,356,862	03/12/02	Bailey	703	16	09/24/98
<i>Appl</i>	F	6,058,263	05/02/00	Voth	395	500.46	06/03/96
<i>Appl</i>	G	5,999,725	12/07/99	Barbier et al.	395	500.49	04/17/98
<i>Appl</i>	H	6,289,300	09/11/01	Brannick et al.	703	28	02/06/98
<i>Appl</i>	I	6,298,320	10/02/01	Buckmaster et al.	703	28	02/17/98
<i>Appl</i>	J	6,366,878	04/02/02	Grunert	703	28	09/28/98
<i>Appl</i>	K	5,889,988	03/30/99	Held	395	673	11/08/96
<i>Appl</i>	L	6,487,700	11/26/02	Fukushima	716	4	03/08/00
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<i>Appl</i>	N	6,223,272	04/24/01	Coehlo et al.	712	1	07/15/98
<i>Appl</i>	O	5,964,893	10/12/99	Circello et al.	714	39	08/30/95
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<i>Appl</i>	S	5,590,354	12/31/96	Klapproth et al.	395	800	07/28/94
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<i>Appl</i>	U	6,564,179	05/13/03	Belhaj	703	26	07/26/99
<i>Appl</i>	V	5,587,957	12/24/96	Kowalczyk et al.	365	230.03	09/29/95
<i>Appl</i>	W	6,385,742	05/07/02	Kirsh et al.	714	39	03/05/99
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<i>Appl</i>	BB	5,752,013	05/12/98	Christensen et al.	395	568	06/30/93
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<i>Appl</i>	MM	6,223,144	04/24/01	Barnett et al.	703	22	03/24/98	
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<i>April</i>	GGG	Dahl et al., "EMULATION OF THE SPARCLE MICROPROCESSOR WITH THE MIT VIRTUAL WIRES EMULATION SYSTEM"; 1994; IEEE; pages 14-22
<i>April</i>	HHH	Bauer et al.; "A RECONFIGURABLE LOGIC MACHINE FOR FAST EVENT-DRIVEN SIMULATION"; 1998; Design Automation Conference Proceedings; pages 668-671
<i>April</i>	III	Bursky; "FPGA COMBINES MULTIPLE INTERFACES AND LOGIC"; Electronic Design; Vol. 48 No. 20; pp 74-78 (Oct. 2, 2000)
<i>April</i>	JJJ	Anonymous, "WARP NINE ENGINEERING - THE IEEE 1284 EXPERTS-F/PORT PRODUCT SHEET"; undated web page found at http://www.fapo.com/fport.htm
<i>April</i>	KKK	Anonymous; "F/PORT: FAST PARALLELL PORT FOR THE PC: INSTALLATION MANUAL : Release 7.1," circa 1997, available for download from http://www.fapo.com/fport.htm
<i>April</i>	LLL	Nam et al. ; "FAST DEVELOPMENT OF SOURCE-LEVEL DEBUGGING SYSTEM USING HARDWARE EMULATION"; IEEE 2000; pages 40-404
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<i>April</i>	OOO	Oh et al.; "EMULATOR ENVIRONMENT BASED ON AN FPGA PROTOTYPING BOARD"; IEEE 21-23; June 2000; pages 72-77
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<i>April</i>	QQQ	Ching et al.; "AN IN-CIRCUIT EMULATOR FOR TMS320C25"; IEEE 1994; pages 51-56
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<i>April</i>	VVV	Sedory; "A GUIDE TO DEBUG"; 2004' retrieved on 5/20/05
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<i>April</i>	XXX	Anonymous; "USING DEBUG"; 1999; Prentice-Hall Publishing; pages 1-20
<i>April</i>	YYY	XEROX; MESA DEBUGGER DOCUMENTATION "; April 1979; XEROX Systems Development Department; Version 5.0; pages 1-30
<i>April</i>	ZZZ	Stallman et al.; "DEBUGGING WITH THR GNU SOURCE-LEVEL DEBUGGER"; January 1994; retrieved on May 2, 2005 from http://www.cs.utah.edu ; Stopping and Continuing"
Examiner	<i>April Sharon</i>	
	Date Considered	<i>12/14/05</i>

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered.
Include copy of this form with next communication to applicant.



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U.S. Patent Documents

Examiner Initial	No.	Patent No.	Date	Patentee	Class	Sub-class	Filing Date
<i>Agul</i>	A	6,460,172	10/01/02	Insenser Farre et al.	716	17	06/21/00

Foreign Patent or Published Foreign Patent Application

Examiner Initial	No.	Document No.	Publication Date	Country or Patent Office	Class	Sub-class	Translation	
							Yes	No
<i>Agul</i>	B							

Other Documents

Examiner Initial	No.	Author, Title, Date, Place (e.g. Journal) of Publication
	C	
Examiner	Date Considered	
<i>Agul Sharan</i>	<i>12/14/05</i>	

Examiner: Initial citation considered. Draw line through citation if not in conformance and not considered.
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